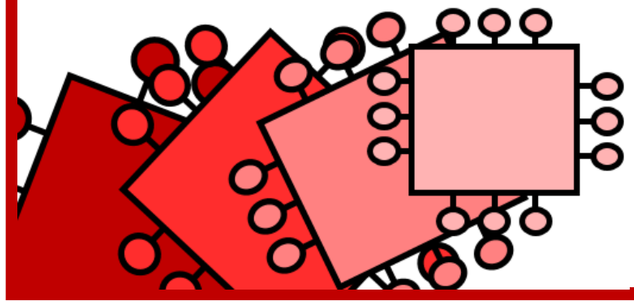
This exemplar Student Learning Record was produced by a Year 12 student from Archway School

SLR 1 – “Structure and function of the processor”

This SLR was graded at B.

Even with A* graded work it is possible to find areas the student can improve or enhance.

NOTE: Students should be encouraged to produce the evidence for their Student Learning Record in any format they wish. This could be directly in the word document as electronic evidence, in traditional pen and paper format, or indeed in any other format such as a Power Point, Prezi or even a video! The important thing here is to assess the quality and depth of the evidence presented, not prescribe a set format.



Busses: Busses are Communication channels between the CPU and the memory. Some are

Busses

Address Bus

Memory

(CPU)

Control Bus

Data Bus

Control bus:

Sends control signals between component and processer (bidirectional bus)

Address bus:

Carries address of instruction or data from MAR to memory (Unidirectional)

Data bus:

Carries data between the processor and memory (can carry instructions too)

ALU: The part of the CPU that does arithmetic and logical comparisons

PC: The part of the CPU that stores the address of next instruction.

Control Unit: The part of the CPU that sends signals, controls how data moves around the CPU and to the RAM

MAR: Part of the CPU that stores address of data or instructions to be sent to or fetched from the memory

MDR: Part of the CPU that stores data to be sent to or fetched from the memory

CIR: The part of the CPU that Stores instruction that is being decoded.

ACC: The part of the CPU that stores results of calculations from the ALU

1

Arithmetic Logic unit

Current Instruction Register (CIR)

R0

R1

Program Counter (PC)

Status register (SR)

Control Unit

Memory Address Register (MAR)

Memory Data Register (MDR)

2

Arithmetic Logic unit

Current Instruction Register (CIR)

R0

R1

Program Counter (PC)

Status register (SR)

Control Unit

Memory Address Register (MAR)

Memory Data Register (MDR)

External Bus

Main Memory

3

Arithmetic Logic unit

Current Instruction Register (CIR)

R0

R1

Program Counter (PC)

Status register (SR)

Control Unit

Memory Address Register (MAR)

Memory Data Register (MDR)

External Bus

Main Memory

Fetch-decode-execute cycle

Fetch

- The PC always holds the address of the next instruction to be done.
- The address then gets copied to the MAR.
- It is also copied to the MDR.
- Whatever is in the MDR then gets copied to the CIR and the PC is incremented.

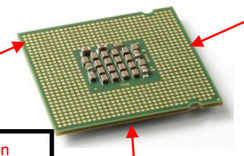
Decode

- Whatever is held in the CIR is split into a binary code (the operation to be carried out) and the address of the data that needs to be used.
- The control unit interoperates the operation code and lets the processor know what needs to happen next.

Executer

- The CIR copies the address part of the instruction.
- The data in the MAR is copied to the MDR.
- The data is used.

Central processing unit (CPU)



Clock speed: The clock speed is measured in hertz (Hz), it's a constant frequency that the internal clock generates using a piece of quartz. If there is a faster clock rate then the computer can work faster. The clock unit synchronises the other components with a regular pulse.

Cores: A core is an independent CPU. It can be part of a 'multi core processor' that has multiple cores all working simultaneously. Doubling the number of cores will not however double the processing power, as some of this is needed to run the cores.

Cache: The cache lives in the CPU and is a really fast piece of memory that works in megabytes.

Fetch decode execute: The cycle in which an address for an instruction is fetched by an address bus and then sent by the data bus to be separated into binary code for the address and operation to be done. Then decoded by the Control unit.

CPU: The central processing unit is the main part of the computer and holds the registers, control unit and ALU.

CPU

Control Unit

Arithmetic Logic Unit

Main Memory (RAM)

Main memory

Fetch

CPU Program Counter

Decode

Load data

Store data in memory

Execute logical or arithmetic operation

Execute

Harvard architecture: In Harvard architecture there are two system busses between a CPU and two rams, one with memory and the other with instructions.

Memory (Instructions)

Control unit

Memory (Data)

Von Neumann Architecture: This is a traditional type of architecture. It is composed of a linear fetch-decode-execute cycle that is managed by a single control unit.

Examination Questions

5 The program, as shown in Fig.2 below, is written in assembly code using the Little Man Computer instruction set. It is *supposed* to take in two numbers and output the higher.

```
        INP
        STA   NUMA
        INP
        STA   NUMB
        SUB   NUMA
        BRP   NOTA
        LDA   NUMB
        BRA   QUIT
NOTA    LDA   NUMA
QUIT    OUT
        HLT

NUMA    DAT
NUMB    DAT
```

A processor executes this program following the Fetch-Decode-Execute cycle. To do this it needs to make use of registers.

One of the registers used is the Program Counter (PC). Ordinarily it would be incremented by one each cycle.

(e)

(i) Identify an instruction in the Little Man Computer program shown in Fig.2 that would cause the PC to change in a different way.

.....[1]

(ii) State which register the contents of the PC would be copied to in order for the processor to access the next instruction.

.....[1]

(c) (i) Describe the fetch-execute cycle.

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1 - Structure and function of the processor (AS / A Level)

Specification Points / Learning Objectives:

Core text book page ref: 124-131, 133-134

AS Level	A Level	Specification point description
1.1.1a	1.1.1a	The arithmetic logic unit; ALU, Control Unit and Registers (Program Counter; PC, Accumulator; ACC, Memory Address Register; MAR, Memory Data Register; MDR, Current Instruction Register; CIR). Busses: data, address and control: How this relates to assembly language program
1.1.1b	1.1.1b	The fetch-decode-execute cycle, including its effect on registers
1.1.1c	1.1.1c	The factors affecting the performance of CPU, clock speed, number of cores, cache
	1.1.1d	The use of pipelining in a processors to improve efficiency
1.1.1d	1.1.1e	Von Neumann, Harvard and contemporary processor architecture

Expectations / Learning Outcomes:

- Terms 1-21 from your **A Level Key Terminology** PowerPoint should be included and underlined.
- You must include at least one diagram which depicts the fetch-decode-execute cycle.
- You must include at least one diagram which shows the direction and connections of the 3 busses.
- You must include at least one diagram which illustrates how the various registers interact during a typical fetch-decode-execute cycle.

Grade	TG.	Breadth	Depth	Presentation	Understanding
A/A*		ALL	**LINK / FORMULATE** Create, Generate, Hypothesis, Reflect, Theorise, Consider	Quad Core	Quad Core
B/C		MOST	**EXPLAIN / ANALYSE** Apply, Argue, Compare, Contrast, Criticise, Relate, Justify	Dual Core	Dual Core
D/E		SOME	**DESCRIBE / IDENTIFY** Name, Follow Simple Procedure, Combine, List, Outline	Single Core	Single Core
U		FEW	Very little depth of understanding shown		
			MY ASSESSMENT GRADE IN THIS TOPIC IS:		

How To Improve:

My Response Is: (Set yourself specific targets / objectives as to how you will achieve your HTI)

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